REMARKS

In the Office Action dated September 16, 2003, claims 1-27 are noted as pending. Claims 23-27 are rejected under 35 USC 102(e) as being anticipated by Ayukawa et al., U.S. Patent No. 6,381,671 (hereinafter Ayukawa). Claims 1-7 are rejected under 35 USC 103(a) as being unpatentable over Saulsbury et al., U.S. Patent No. 6,128,702 (hereinafter Saulsbury) in view of Ayukawa. Claims 6-9 are rejected under 35 USC 103(a) as being unpatentable over Saulsbury in view of Westberg et al., U.S. Patent No. 5,361,391 (hereinafter Westberg). Claims 10-14 and 17-21 are rejected under 35 USC 103(a) as being unpatentable over Saulsbury in view of Westberg and in further view of Ayukawa.

Objections to the Specification

The specification has been amended to cure the informality.

REJECTIONS UNDER 35 U.S.C. 102(b)

Applicant requests cancellation of claims 23-27.

REJECTIONS UNDER 35 U.S.C. 103(a)

Neither Saulsbury, nor Westberg, nor Ayukawa, either individually or in combination, disclose a data cache located on a memory module controlled by a command sequencer and serializer unit where the "command sequencer and serializer unit to reduce a first plurality of address and command signals down to a more narrow set of signal lines coupled to the memory module, the more narrow set of signal lines forming a

point-to-point interconnect between the command sequencer and serializer unit and the memory module" as claimed in amended claim 1. It should be noted that the command sequence and serializer unit and array of tag addresses are not located on the memory module, as indicated by the language of claim one describing an interconnect coupling the command sequencer and serializer unit to the memory module. The tag array, data cache, and memory bank in Saulsbury are all located on the same component, and there is no teaching of a serializer unit with the limitations claimed in claim 1. Further, claim 1 provides "the command sequencer and serializer unit to cause a current line of data to be read out of a memory module memory device and to load a next line of data from the memory module memory device to the data cache" which is also not taught by a combination of the cited references. For these reasons, claim 1 is patentable over the cited references.

Further, a combination of the Saulsbury, Westberg, and Ayukawa references would not yield a memory module including a data cache that is controlled by a memory controller including an array of tags where the memory controller is not located on the memory module (the memory controller controls the memory module via a memory bus), as claimed in amended claim 8. Claim 8 also cites a plurality of commands including a read and preload command to cause a current line of data to be read out of the memory device and to load a next line of data from the memory device to the data cache.

Similarly, the cited references in combination would not yield all of the limitations of claim 15 which includes limitations similar to those in claims 1 and 8, discussed above.

CONCLUSION:

In view of the foregoing, Applicants submit that claims 1, 3-8, 11-16, and 18-22 are distinguished over the cited art and are in condition for allowance. Allowance of claims 1, 3-8, 11-16, and 18-22 is respectfully requested.

DEPOSIT ACCOUNT AUTHORIZATION

Authorization is hereby given to charge our Deposit Account No. 02-2666 for any additional charges that may be due.

Respectfully submitted,

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